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ENHANCED CHIP SCALE PACKAGE FOR WIRE BOND DIES

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ENHANCED CHIP SCALE PACKAGE FOR WIRE BOND DIES

BACKGROUND OF THE INVENTION

The present invention generally relates to integrated circuits, and particularly relates to chip scale packaging of wire bonded integrated circuits.

Packaging technology represents an enabling element in the ongoing microelectronics revolution. As integrated circuits have shrunk, so too have the physical packages carrying these devices. Various techniques are used to minimize the physical space required for integrated circuits, and to accommodate the increasingly high number of signal connections associated with dense integrated circuit devices.

Common approaches include various chip-on-glass and chip-on-board technologies. In these, an integrated circuit die is mounted directly on a primary circuit substrate, covered only by a minimal amount of epoxy or resin. While offering certain advantages in high-volume manufacturing environments, integrated circuit devices of this nature place significant challenges on handling and testing.

Other approaches strike a balance between physical size and the practical considerations of handling and testing. So-called "chip scale packages" (CSPs) attempt to provide physical packaging for integrated circuit die without increasing the total physical size substantially beyond that of the actual die. Ideally, such packages remain as small as possible while still providing relatively robust protection for the die itself.

Chip scale packaging techniques may incorporate wire bond technology. With wire bond technology, fine wire bonds taken from signal connection points on the die are arrayed as “flying leads,” usually around the perimeter edges of the die. These wire bonds are bonded to corresponding connection points, such as wire bond fingers, on the top surface of a chip carrier on which the die is mounted.

The chip carrier functions much like a printed circuit board, providing a rigid (or sometimes flexible) platform that can be readily handled and more easily mounted to a

larger circuit board carrying other electrical or electronic circuits. Essentially, the chip carrier provides practical access to the electrical interconnections of the die it carries.

Typically, the chip carrier comprises a substrate with a top layer providing signal and ground connections for interconnecting with corresponding electrical connections on the die. The carrier's bottom side usually carries corresponding connection points, which may be soldered to corresponding connections on the primary circuit board. Generally, these connection points carry solder balls, allowing the carrier to be reflow soldered to the primary circuit board.

While such CSPs maintain a small overall size, they are not without potential disadvantages. For example, the overall electrical impedance between the die's signal points and corresponding connections on the primary circuit board can be undesirably high, contributing to signal degradation and limiting upper operating frequencies. Also, such CSPs may offer poor thermal conduction between the die and the primary circuit board, thus limiting the amount of power that may be dissipated in the die.

BRIEF SUMMARY OF THE INVENTION

A chip scale package assembly comprises an integrated circuit die wire bonded to a carrier. The carrier provides for electrical interconnection with the die and is suitable for mounting on a primary circuit board. Wire bond fingers on the top of the carrier are arrayed around the die mounting area and provide connection points for the die's bond wires, which points are generally grouped in rows along each edge of the carrier. A ground plane surrounds these groups of connection points and also covers the die mounting area. Thermal vias in the die mounting area electrically and thermally couple the ground plane to a second ground plane on the bottom of the carrier. That ground plane includes ground pads with attached solder balls for connection with the primary circuit board. Similarly, signal vias couple the wire bond fingers to corresponding signal

pads on the bottom of the carrier, the pads of which also carry solder balls for attachment to the primary circuit board.

By providing a top-side ground plane covering the die mounting area, die grounding is accomplished through mounting the die in electrical connection with the ground plane. This eliminates the need for using one or more bond wire connections to ground the die. Thus, all bond wires may be dedicated to signal connections. Surrounding the bond wire finger terminations for all of these signal connections with the top-side ground plane enhances signal integrity by minimizing cross-talk and ground loop area. Further, positioning thermal vias in the top-side ground plane generally within the die mounting area provides low thermal and electrical impedance connections between the top and bottom side ground planes. The ground pads with attached solder balls on the bottom side ground plane complete the low thermal and electrical impedance connections between the die and the primary circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified side view of an exemplary chip scale package assembly in accordance with the present invention.

Fig. 2 is diagram of the top metal layer of the carrier shown in Fig. 1.

Fig. 3 is a diagram of the bottom metal layer of the carrier shown in Fig. 1.

Fig. 4 is a diagram of insertion loss and reflection for an exemplary embodiment of the assembly of Fig. 1.

Fig. 5 is a diagram of modeled and measured signal propagation performance for the assembly of Fig. 1.

Fig. 6 is a diagram of modeled thermal performance for exemplary variations on the assembly of Fig. 1 as compared to a baseline assembly.

DETAILED DESCRIPTION OF THE INVENTION

Turning now to the drawings, Fig. 1 illustrates an exemplary embodiment of the chip scale package assembly of the present invention, generally referred to by the numeral 10. The assembly 10 comprises an integrated circuit die 12, and a chip carrier 14. The carrier 14 provides an interface between the die 12 and a primary circuit board 16.

The die 12 may be essentially any type of integrated circuit (IC) die, whether a digital IC, analog IC, or mixed signal IC, and may be implemented in a wide variety of semiconductor process technologies. The die 12 includes a number of electrical connections on its top side (not shown). These connections, typically for signals, are coupled to the carrier 14 using "bond wires" 18, which are arranged as a set of flying leads around the edges of the die 12. The die 12 further includes one or more ground connections on its bottom side, for making ground connection with the carrier 14. The die 12 is mounted to a top side 26 of the carrier 14, and is protected by a mold compound 20 formed over it. The mold compound 20 covers the die 12, sealing the die 12 against the carrier 14, and providing mechanical and environmental protection for the die 12 and its bond wires 18.

The primary circuit board 16 does not comprise a part of the assembly 10, but is typically part of the environment in which the assembly 10 is used. Generally, the board 16 includes one or more circuit devices that are electrically coupled to one or more signals from the die 12, once the assembly 10 is mounted to the board 16. The bottom side 30 of the carrier 14 includes a number of solder balls 22, which allow the assembly 10 to be soldered to the appropriate connections—generally a set of mounting pads—on the board 16. Typically, this mounting process entails subjecting the board 16 with the mounted assembly 10 to a solder "reflow" process that heats the solder balls 22 enough

to cause them to melt in a controlled fashion, thereby joining with the mounting pads (not shown) on the primary circuit board 16.

The carrier 14 comprises substrate 24, which may be a rigid resin-base laminate with suitable dielectric, mechanical, and thermal properties, such as bismaleimide triazine (BT), or may be some other material with the appropriate characteristics as needed or desired. The substrate 24 has a top side metal layer 28 disposed on the top side 26 of the carrier 14, and a bottom side metal layer 32 disposed on the bottom side 30 of the carrier 14.

Fig. 2 illustrates the top-side metal layer 28. A ground plane 40 generally covers the top side of the carrier 14, and includes a hatched portion 42 positioned within a die mounting area 44 on the top side of the carrier 14. A plurality of connection points 46 are arranged into groups generally along each side of the carrier 14. Preferably, these connection points are wire bond fingers 46, which provide a point of attachment for the bond wires 18 from the die 12. The bond wires 18 carrying signals from the die 12 are soldered to or otherwise connected with the wire bond fingers 46. Each wire bond finger 46 has a corresponding signal via 48 that extends through the substrate 24 and provides an electrical connection to a corresponding signal pad (shown later) on the bottom of the carrier 14. The top-side metal layer 28 further comprises a plurality of grounded thermal vias 52.

The ground plane 40 is electrically isolated from the wire bond fingers 46 and the signal vias 48, but completely surrounds each group of wire bond fingers 46 and associated signal vias 48 in the top side metal layer 28. The continuous border formed in the ground plane 40 around each group conforms to the contours defined by the arrangement of fingers 46 and vias 48 within each group. By conforming to these defined contours, the ground plane 40 is maintained in close proximity to the signal interconnections (e.g., bond wire fingers 46) between the carrier 14 and the die 12.

Preferably, the ground plane 40 comprises a metallic plane, such as a copper foil for example.

While configuring the ground plane 40 to have a close-proximity, contoured border surrounding all signal connections made on the top side metal layer 28 enhances signal integrity, incorporating the hatched portion 42 within the die mounting area 44 enhances mechanical reliability. Hatching improves reliability for a number reasons, including enhancing the thermal expansion characteristics of the plane 40 in the area immediately beneath the die 12.

The grounded thermal vias 52 also contribute to electrical signal integrity by providing low electrical impedance connections from the top side 26 of the carrier 14 to its bottom side 30. The grounded thermal vias 52 also contribute to the enhanced thermal performance of the assembly 10 by providing thermal conduits beneath the die 12 to the bottom side 30 of the carrier 14. Thermal energy conducted away from the die 12 and down through the thermal vias 52 can be transferred to the primary circuit board 16, which can incorporate heat dissipation features, such such as its own ground planes.

The grounded thermal vias 52 are generally positioned within the die mounting area 44, although the actual die mounting area 44 may be somewhat smaller, in which case the thermal vias 52 would be positioned generally along the perimeter edges of the die 12. In either case, it is expected that the die 12 includes one or more ground connections positioned on its bottom side such that the die 12 is electrically grounded once mounted in contact with the ground plane 40.

Fig. 3 illustrates the bottom metal layer 32, which comprises a ground plane 60, ground pads 62 positioned within the ground plane 60, signal pads 64 generally arrayed around the ground plane 60 along the perimeter edges of the carrier 14, and plating bars 66. The plating bars 66 facilitate plating, such as with a tin-lead overlay, of the various metallic features on the bottom side 30 of the carrier 14. All or a portion of the plating

bars may be removed subsequent to plating operations.

Note that the thermal vias 52 positioned within the ground plane 60 correspond to those thermal vias 52 shown in Fig. 2. Similarly, the signal vias 48 interspersed among the signal pads 64 correspond to the signal vias 48 shown in the top-side metal layer 28. Conductive traces 65 couple respective signal pads 64 to corresponding signal vias 48.

Each wire bond finger 46 on the top side 26 couples to a corresponding signal via 48, which is in turn coupled with a corresponding one of the signal pads 64 on the bottom side 30. Each signal pad 64 carries a solder ball 22 for attachment with a corresponding connection (not shown) on the primary circuit board 16. Thus, each bond wire connection 18 from the die 12 is electrically coupled to the corresponding primary circuit board connection through the carrier 14. Also, the grounded thermal vias 52 provide electrical and thermal coupling between ground plane 40 on the top side 26 and ground plane 60 on the bottom side 30. As with ground plane 40, ground plane 60 preferably comprises a metallic plane, such as copper foil.

The ground pads 52 positioned within the ground plane 60 each carry a solder ball 22 for attachment to a corresponding ground connection (not shown) on the primary circuit board 16. The interconnected ground planes 40 and 60 and the solder balls 22 attaching the ground pads 62 with the primary circuit board 16 provide low impedance electrical and thermal bonding between the die 12 and the primary circuit board 16. The number of solder ball attachments between the ground plane 60 and the primary circuit board 16 influences the thermal impedance seen by the die 12 with respect to the primary circuit board 16.

Too few ground pads 62 might result in undesirable heat build-up in the die 12, particularly where the die 12 is a high-power device. However, adding ground pads 62 beyond a reasonable number results in only incremental thermal improvements.

Something in the range of twenty-eight ground pads 62 providing twenty-eight solder ball connections with the primary circuit board 16 is an exemplary configuration, although more or fewer may be used as needed or desired.

Figs. 4, 5, and 6 depict various aspects of electrical and thermal performance for an exemplary embodiment of the assembly 10. In this embodiment, the assembly 10 comprises a 7 mm x 7 mm square carrier 14 employing twenty-eight bottom-side ground pads 62 coupled to the primary circuit board 16 through corresponding solder balls 22, and thirty-two grounded thermal vias 52 coupling ground planes 40 and 60. The solder balls 22 are implemented with a 0.5 mm pitch (ball-to-ball spacing).

Fig. 4 illustrates the modeled high frequency characteristics of the assembly 10 in terms of insertion loss (upper graph line) and reflection loss (lower graph line), measured in dB and plotted from one to ten GHz. The modeled performance is based on a two-port model, and is taken across an opposing pair of wire bond fingers 46 on the exemplary assembly 10.

Fig. 5 illustrates measured performance in the time domain taken from an assembly 10 built in accordance with the above details. The graph plots voltage against time for output signals edges (B) and (C) with respect to an injected (input) signal edge (A). Graph line (B) depicts the modeled (estimated) response of the assembly 10, while graph line (C) depicts actual, measured response. As may be seen, the actual output signal edge in graph line (C) exhibits little delay and essentially no ringing with regard to the input edge in graph line (A).

Fig. 6 illustrates the thermal performance of the assembly 10 for twenty-eight and sixty-four ground pads 62 (with attached solder balls 22) as compared to a base line package assembly that is similar but lacks ground pads 62, thermal vias 52, and bottom-side ground plane 60. As seen, the thermal impedance of the exemplary package 10 is significantly lower for both the twenty-eight and sixty-four ground pad configurations,

with the latter being slightly better than the former. For the same type of die 12 under the same operating conditions, the exemplary assembly 10 reduces die junction temperature by approximately 20 °C. The thermal simulation of the package model has been validated with measurements and the designed package can dissipate 2.4 Watts of power under industry-standard test conditions and thermal window.

As discussed above and illustrated in the accompanying drawings, the inventive chip scale package assembly 10 provides enhanced electrical and thermal performance, allowing reliable and sustainable operation of higher-performance dies 12, while maintaining a small package size. The present invention may, of course, be carried out in other specific ways than those herein set forth without departing from the spirit and essential characteristics of the invention. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive, and all changes coming within the meaning and equivalency range of the appended claims are intended to be embraced therein.